USN | | | | | | | | | | |

10ES33

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. Using K – map technique, simplify the following and implement using gates :
i) $f(a\ b\ c\ d) = \Sigma m\ (1, 3, 7, 11, 15) + \Sigma d(0, 2, 4)$.
ii) $f(a\ b\ c\ d) = \Pi m(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$. **(10 Marks)**

b. The input to a control circuit is a 4 – bit binary number $x_3\ x_2\ x_1\ x_0$. Design a logic circuit with minimum number of gates if
i) Output $y_1 = 1$ if input binary number is ≤ 5.
ii) Output $y_2 = 1$ if input binary number is ≥ 9. **(10 Marks)**

2 a. Using Quine – Mc Cluskey method, simplify :
$f(a\ b\ c\ d) = \Sigma m\ (0, 1, 3, 7, 8, 9, 11, 15)$ and determine essential prime implicants. **(10 Marks)**

b. What are the advantages of Map – Entered Variable (MEV) method? Illustrate MEV method for $f = \Sigma m\ (0, 1, 4, 7)$. Verify your answer using 3 – variable K – map method. **(10 Marks)**

3 a. Explain the General structure of a decoder. Construct 4 × 16 line decoder using 3 × 8 decoder. Explain its working. **(12 Marks)**

b. Design and implement an octal to binary encoder using minimum number of gates. **(08 Marks)**

4 a. Implement the following function using
4 × 1 MUX : $f(a, b, c, d) = \Sigma m\ (0, 1, 2, 4, 6, 9, 12, 14)$. **(08 Marks)**

b. Construct 1 × 8 demultiplexer using 1 ×4 demultiplexer. **(05 Marks)**

c. Design a BCD adder using 4 bit binary adder. Draw the logic circuit. **(07 Marks)**

PART - B

5 a. Compare combinational circuit with sequential circuit. **(05 Marks)**

b. Explain the principle of Bistable element. **(05 Marks)**

c. Explain the master slave JK flip flop with input and output waveforms. **(10 Marks)**

6 a. What is a Shift Register? Explain the working of the serial – in - serial – out shift register. **(10 Marks)**

b. Design a mod – 6 counter using clocked SR flip flop. **(10 Marks)**

7 a. Explain the principle of Moore model and Mealy model. **(10 Marks)**

b. Analyse the synchronous sequential circuit shown in fig. Q7(b). **(10 Marks)**

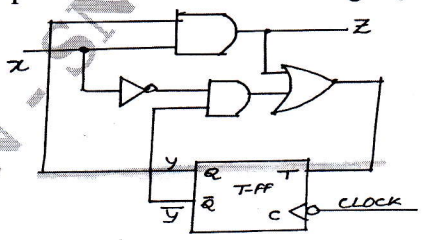

Fig.Q7(b)

8 a. Design a synchronous decade counter using T – Flip - Flops. Draw the timing diagram also. **(10 Marks)**

b. Design a sequence detector circuit to detect serial input sequence of 101 using Mealy model. **(10 Marks)**

*****